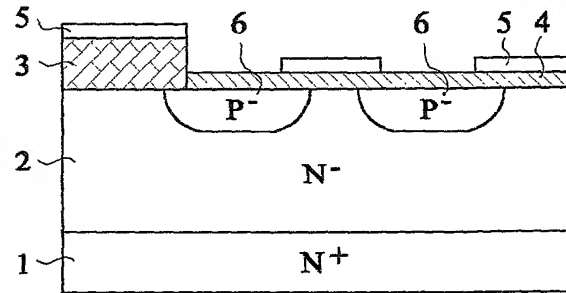
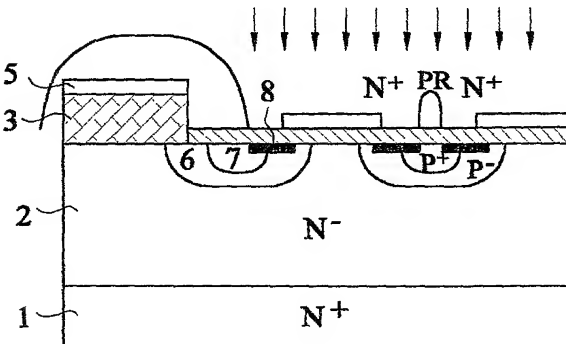


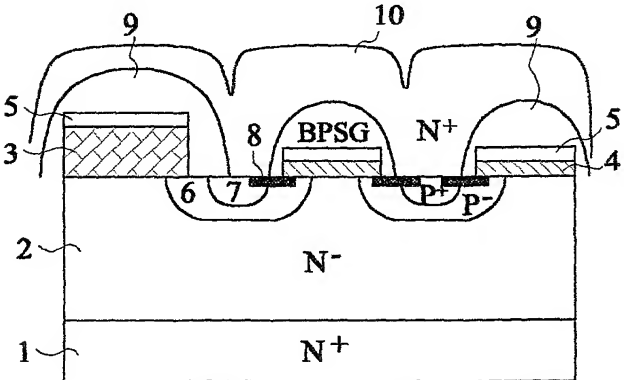
(b)



(d)

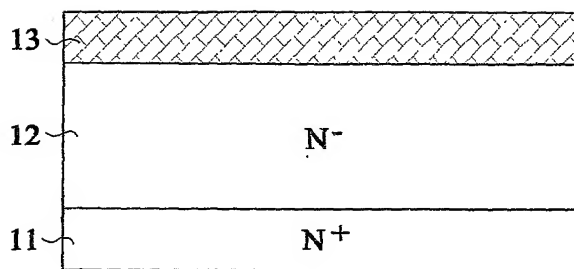


(f)

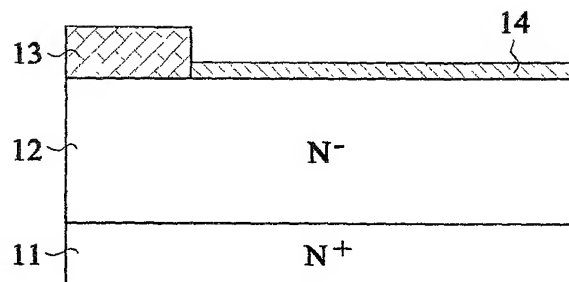


(h)

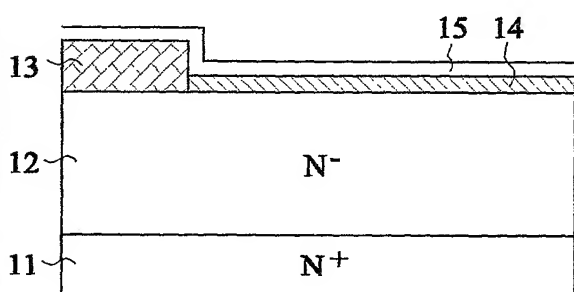
FIG. 1



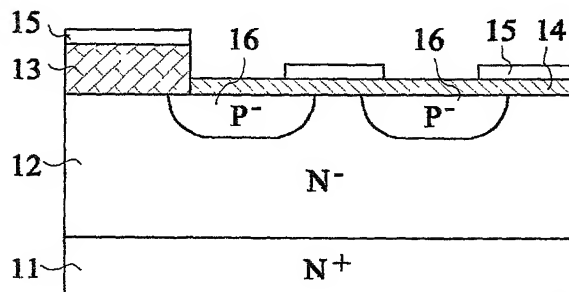
(a)



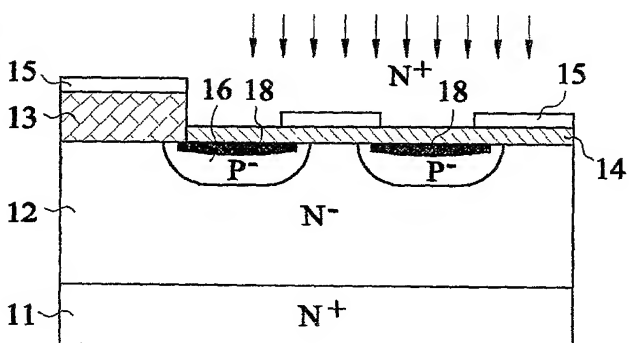
(b)



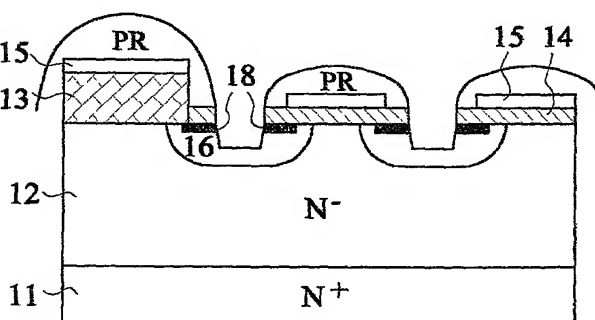
(c)



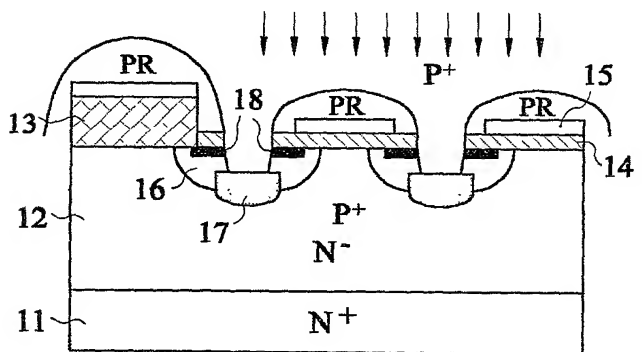
(d)



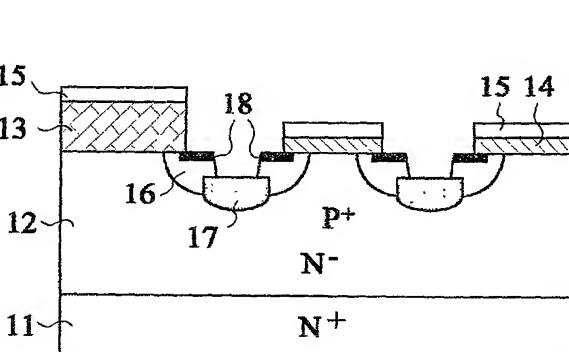
(e)



(f)

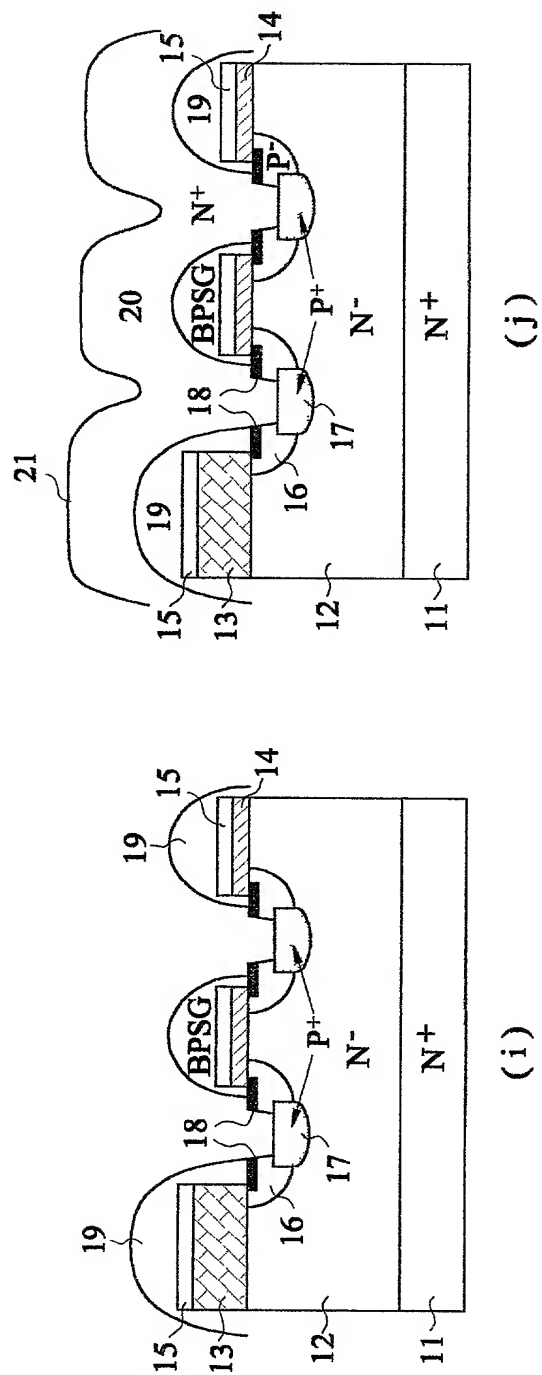


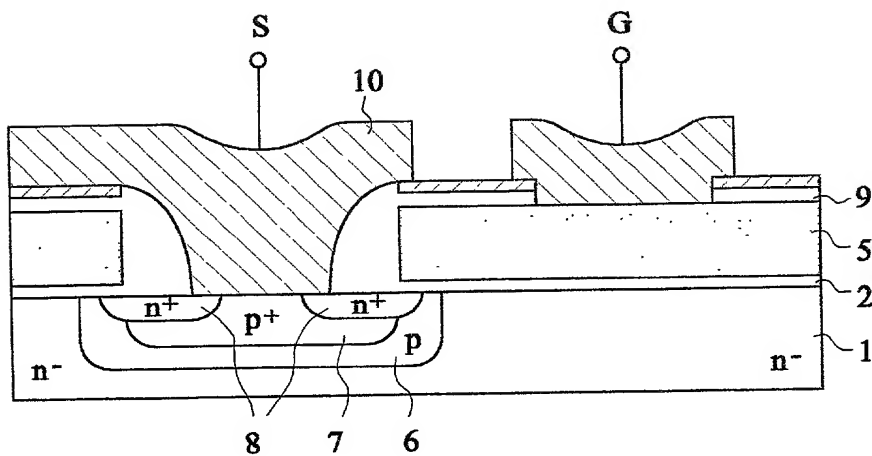
(g)



(h)

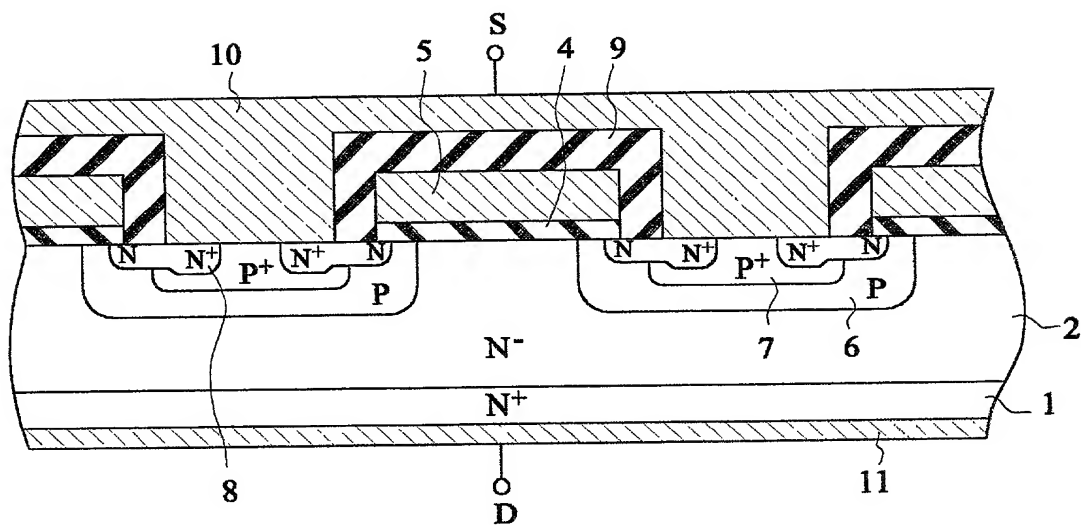
FIG. 2





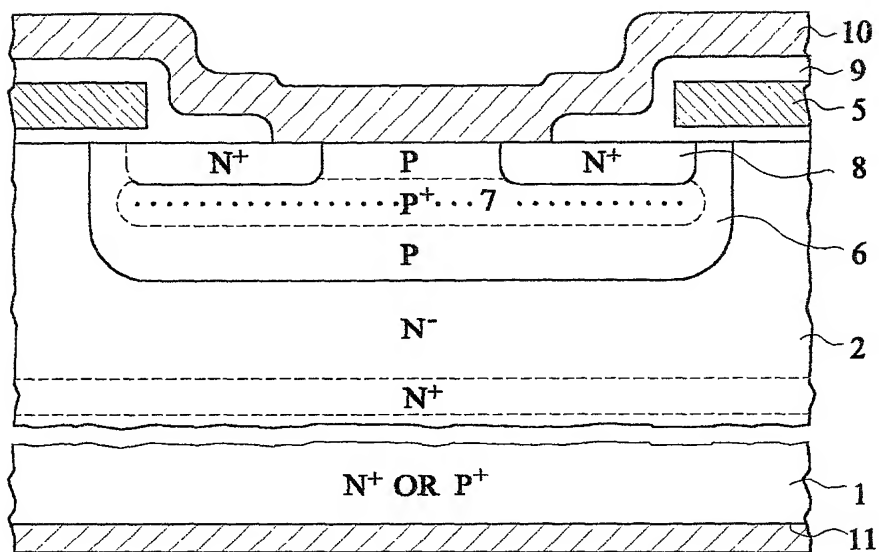
(PRIOR ART)

FIG. 3



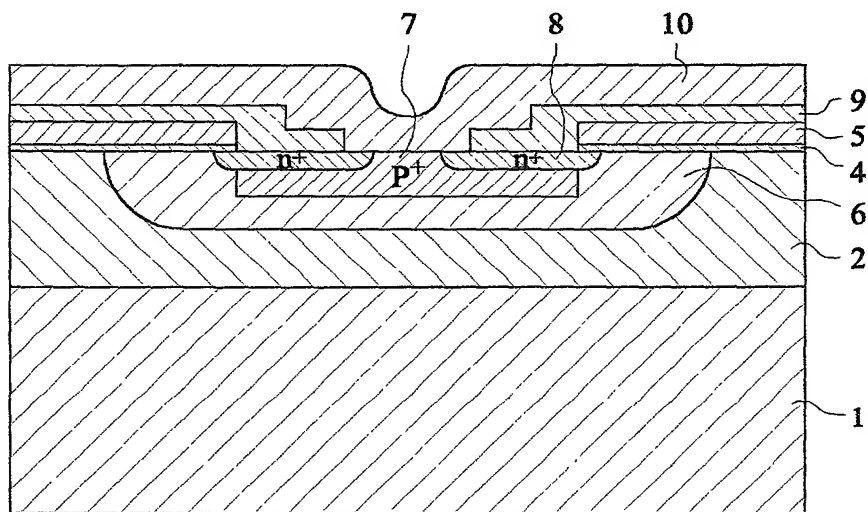
(PRIOR ART)

FIG. 4



(PRIOR ART)

FIG. 5



(PRIOR ART)

FIG. 6

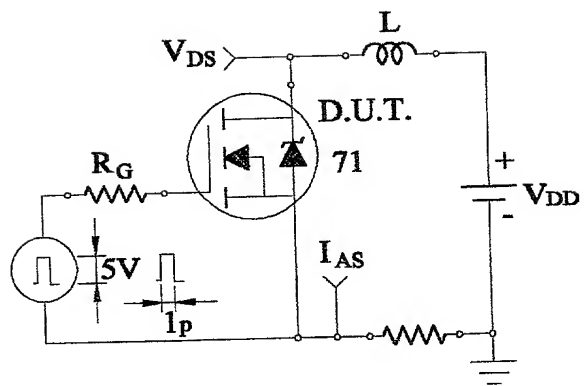


FIG. 7a

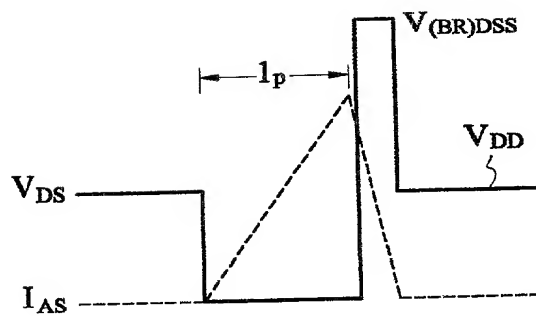


FIG. 7b

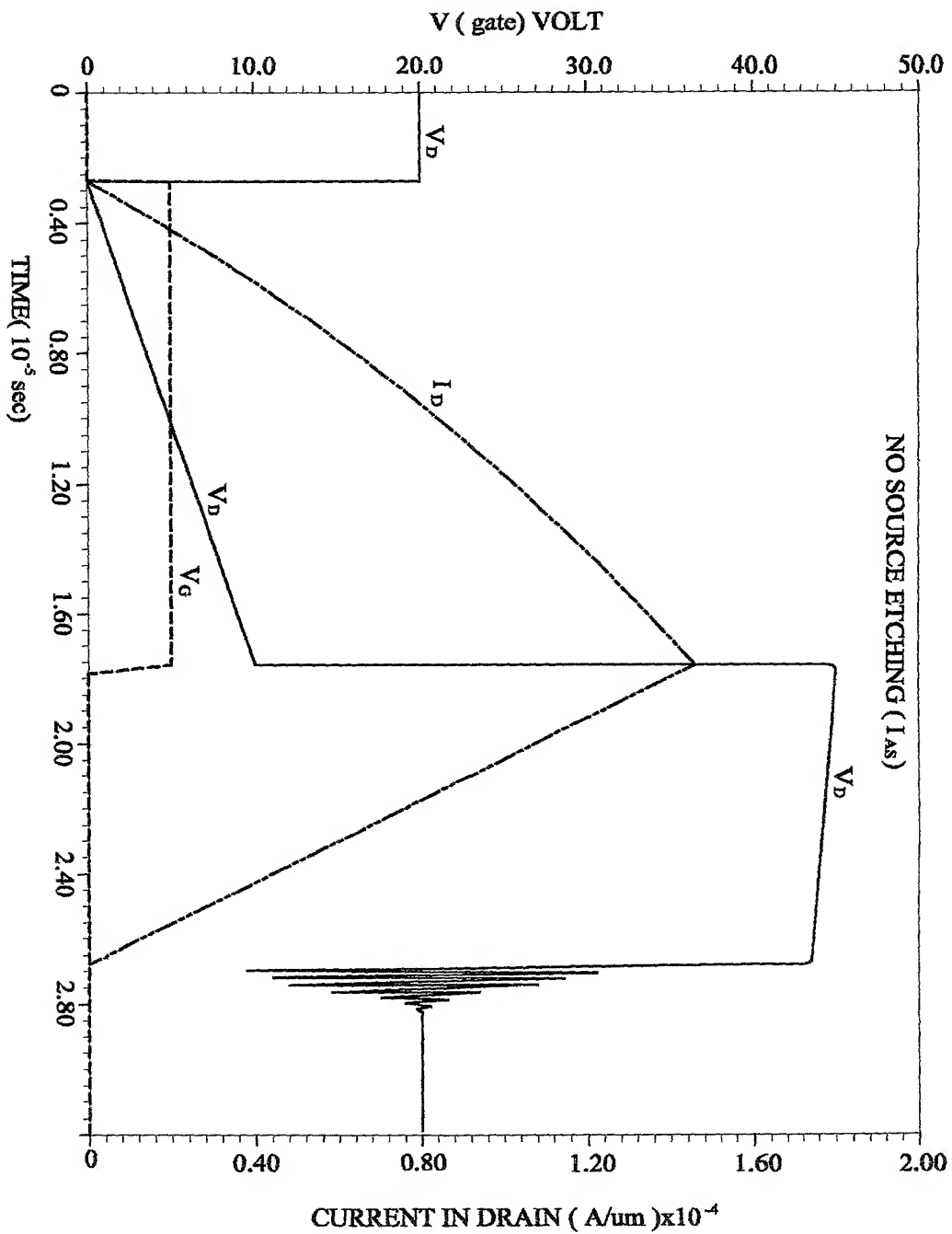


FIG. 8 (PRIOR ART)

FIG. 8 (PRIOR ART) is a graph showing the relationship between the gate voltage (V<sub>G</sub>), the drain current (I<sub>D</sub>), and the drain voltage (V<sub>D</sub>) for a device with no source etching. The x-axis represents time in units of 10<sup>-5</sup> seconds, ranging from 0 to 2.80. The y-axis represents the gate voltage (V<sub>G</sub>) in volts, ranging from 0 to 50.0. The graph shows a ramp-up of V<sub>D</sub> and I<sub>D</sub> from 0 to 2.00, followed by a plateau at V<sub>D</sub> = 20.0 V and I<sub>D</sub> = 1.60 A/um × 10<sup>-4</sup> until 2.40, and then a ramp-down to 0 at 2.80. V<sub>G</sub> is shown as a dashed line, remaining at 0 V throughout the time interval.

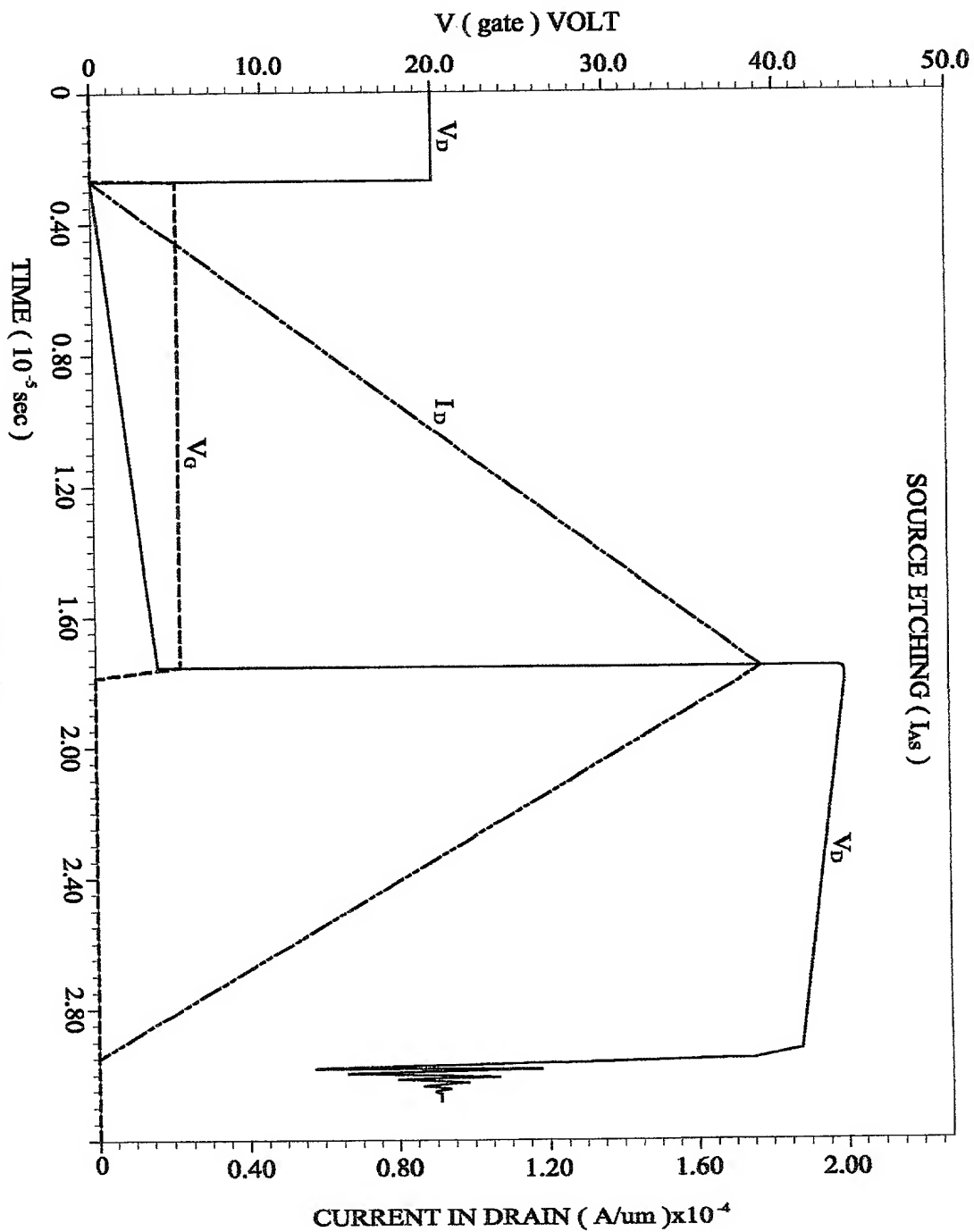


FIG. 9